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08SCS21

Second Semester M.Tech. Degree Examination, May/June 2010
Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain any four dimensions of an instruction set architecture. **(05 Marks)**
b. Explain the trends in technology and trends in power in integrated circuits. **(10 Marks)**
c. State and explain Amdahl's law. **(05 Marks)**

2 a. Explain with a neat diagram, the classic five stage pipeline for a RISC processor. Explain a pipeline showing the pipeline registers between successive pipeline stages. **(10 Marks)**
b. With neat diagrams, explain structural and data hazards. **(10 Marks)**

3 a. With a neat diagram, explain the basic pipeline for MIPS. **(08 Marks)**
b. Explain dynamic branch prediction and branch prediction buffers with neat diagrams. **(04 Marks)**
c. Explain the basic structure of a MIPS floating point unit, using Tomasulo's algorithm. **(08 Marks)**

4 a. With neat diagrams, explain branch target buffers and steps involved in handling an instruction with a branch target buffer. **(10 Marks)**
b. Explain five levels of branch prediction. **(10 Marks)**

5 a. Explain with diagrams, the basic structure of a centralized shared memory multiprocessor and the basic architecture of a distributed memory multiprocessor consisting of individual nodes containing a processor, memory and I/O. **(12 Marks)**
b. Explain the cache coherence problem. Discuss snooping protocols with examples. **(08 Marks)**

6 a. Explain the write invalidate cache coherence protocol for a write back cache with its state transitions based on requests from CPU and requests from the bus. **(10 Marks)**
b. Explain synchronization with respect to basic hardware primitives and implementing locks using coherence. Give examples. **(10 Marks)**

7 a. Assume we have a computer where the clocks per instruction (CPI) is 1.0, when all memory accesses hit in the cache. The only data accesses are loads and stores and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instructions were cache hits? **(06 Marks)**
b. Mention the six basic cache optimizations. **(06 Marks)**
c. Explain any four advanced optimizations of cache performance. **(08 Marks)**

8 a. Draw the data flow graph for computing cos x, where $\cos x \simeq 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \frac{x^6}{6!}$. **(04 Marks)**
b. Explain a typical VLIW processor and instruction format with neat diagrams. Draw and explain VLIW execution with degree = 3. **(08 Marks)**
c. With a neat diagram, explain typical super scalar RISC processor architecture consisting of an integer unit and a floating point unit. **(08 Marks)**

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